# Two-Dimensional Electron Gas Charge-Coupled Devices (2DEG-CCD's)

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*Abstract*—**The two-dimensional electron gas charge-coupled device (2DEG-CCD) structure for III–V and other heterojunction materials is reviewed. Device design considerations for gate, insulator, and channel material parameters are presented. Optimization of 2DEG-CCD performance parameters such as well capacity, dark current, and transfer efficiency is discussed. Experimental results on AlGaAs/GaAs uniform-doped and planar-doped devices are reviewed.**

## I. Introduction

THE two-dimensional electron gas charge-coupled device (2DEG-CCD) structure is an outgrowth of recent advances in 2DEG-FET structures for digital logic circuitry and microwave devices. The 2DEG-FET structures, which are known by several acronyms such as HEMT, SDHT, TEGFET, HIGFET, and MODFET, utilize the abrupt heterointerface between two semiconductor materials and consequent conduction band discontinuity to confine electrons [1]. Due to confinement in the direction perpendicular to the interface, the resultant electron distribution is known as a two-dimensional electron gas. Because of the confinement dimensions and the low electron effective mass usually associated with group III–V materials, quantum mechanics plays an important role in broadening the spatial electron distribution and defining allowed energy states. However, quantum effects typically play a minor role in understanding device behavior at temperatures above 77 K. 2DEG-FET devices have several attributes which include very high mobility of the channel charge (typically in excess of 5000 $cm^2/V \cdot s$ at room temperature), high transconductance, and low voltage-swing requirements.

The 2DEG structure is attractive for CCD applications for several reasons. First, the high low-field mobility and use of a semi-insulating substrate suggest very high speed device operation. Second, the charge handling capability of the 2DEG-CCD structure is large compared with MESFET-type CCD's, and can exceed $1 \times 10^{12}$ carriers/$cm^2$. Third, the lattice-matched heterointerface has a potentially lower interface trap density than the intrinsically mismatched silicon–silicon dioxide interface, as well as improved radiation hardness. Finally, the useful operating temperature of the 2DEG-CCD is expected to be lower than that of the silicon CCD. Other features of the 2DEG-CCD include fabrication compatibility with high-performance, low-noise 2DEG-FET output circuitry and an anti-blooming gate structure.

The 2DEG-CCD differs considerably from MESFET-type GaAs CCD's, which have been shown to operate at frequencies up to 4 GHz with CTE of 0.999 at 1 GHz [2], [3]. Unlike the 2DEG-CCD which is a surface-channel device, the MESFET-type CCD utilizes a buried, doped channel for charge confinement and transport. The Schottky gate is typically deposited directly on the GaAs, though an intermediate layer of AlGaAs has been shown to substantially reduce dark current [3], [4]. Because of the buried channel, the MESFET-type GaAs CCD typically has a charge handling capacity of the order of $1 \times 10^{11}$ carriers/$cm^2$. Impurity and phonon scattering limits the carrier mobility and device speed. At low temperature, $1/f$ noise due to partial impurity freeze-out can limit device dynamic range.

The first fabricated CCD's which attempted to utilize the 2DEG structure were built at Rockwell [5]. However, the fabricated CCD's exhibited poor charge transfer efficiency at room temperature (0.98 at 6 kHz). Since a capacitive-gate structure with open interelectrode gaps (1-$\mu$m size) was used, the CTE would be expected to be non-optimal due to the formation of a potential trough in the interelectrode gap region of the channel. As described by Milano [6], an improved structure for the 2DEG-CCD would be the resistive-gate configuration [7]–[9]. In this structure, a thin-film resistive layer (e.g., 100 k$\Omega/\square$) is used to cover the entire channel region, and narrow metal electrodes are used to apply biases. The resistive gate acts as a continuous voltage divider, leading to a continuously varying channel potential for an empty well. This eliminates the open gap problem and speeds charge transfer by inducing a lateral electric field component, as shown in Fig. 1.

The first resistive-gate 2DEG-CCD was demonstrated by Song *et al.* [10]. This device showed a dramatic improvement in performance with a room temperature CTE of 0.999 in the frequency range of 10 MHz–1 GHz. Performance below 10 MHz was limited by dark current caused by gate leakage. This dark current was later re-

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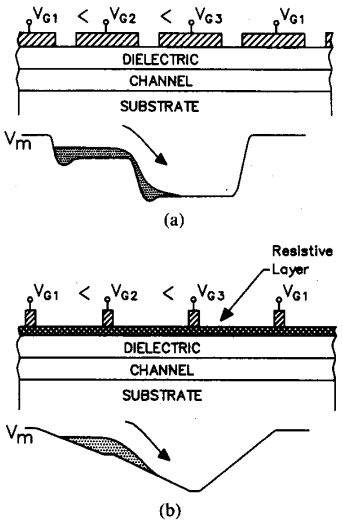



Fig. 1. Schematic cross section of (a) capacitive-gate 2DEG-CCD and (b) resistive-gate 2DEG-CCD.

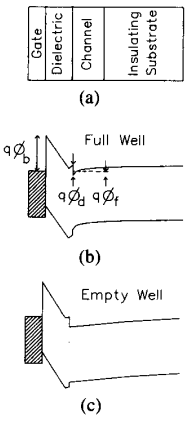



Fig. 2. A generic 2DEG-CCD. (a) Material layer configuration, (b) band diagram for a equilibrium full-well condition, and (c) band diagram for an empty well. The channel layer is undoped and a planar-doped dielectric layer is illustrated.

duced by two orders of magnitude through the use of a planar-doped gate dielectric [11], [12], thus achieving a CTE of 0.9997 in the frequency range 133 kHz–1 GHz. In both cases, the upper frequency range was test station limited.

The 2DEG-CCD has a wide variety of applications. At the high-frequency end of operation, the device is useful for high data rate transient recording (fast-in, slow-out structures), electrooptical signal processing including filtering, and video signal processing. Despite its appeal for high-frequency application, perhaps the greatest potential for the 2DEG-CCD is as a lower frequency imaging detector array multiplexer [13]. This is because of its higher charge handling capability compared to buried-channel silicon devices (without the interface trap noise associated with MOS surface-channel CCD's), and its compatibility with advanced IR detector materials and structures. When realized in the AlGaAs/GaAs system, monolithic image sensors may be possible using photosensitive multiple quantum well (MQW) layers, heterojunction internal photoemission (HIP) layers, or n-i-p-i layers [14]. When used in a hybridized structure, the multiplexer has a thermal expansion coefficient well matched to that of HgCdTe.

This paper reviews the structure and operating principles of the 2DEG-CCD. Device design considerations for gate, dielectric, and channel material parameters are presented. The optimization of 2DEG-CCD performance parameters such as well capacity, dark current, and transfer efficiency is then discussed. Experimental results on AlGaAs/GaAs uniform-doped and planar-doped devices, as well as a two-phase device are reviewed.

## II. Structure and Device Operation

### A. Structure

The structure of the 2DEG-CCD is similar to generic field-effect devices—a gate, a dielectric layer, and a semiconductor channel layer, as shown in Fig. 2(a). In the 2DEG-CCD, the dielectric layer (or insulator) is a semiconductor with a lower electron affinity so that a discontinuity in the conduction band edge at the heterojunction interface confines electrons in the channel layer. Generally, the dielectric material has a wider bandgap than the channel material. The gate material is chosen to achieve a high barrier between the gate and dielectric and minimize leakage current between the gate and channel under biasing. The gate, while usually metal or cermet, may also be a semiconductor, though this has some limitations [15]. To optimize mobility and reduce trapping effects, the channel semiconductor is undoped as is a portion of the dielectric closest to the channel. The latter is often referred to as a dielectric spacer layer. The channel layer is typically grown on a semi-insulating substrate so that field penetration to the backside contact can usually be ignored.

The gate electrodes can be configured either in a capacitive-gate (CG) or resistive-gate (RG) mode. First, the CG mode is described. At low frequency, the CG structure dissipates less power than the RG structure. Electrodes are spaced by gaps in the material and the gap gives rise to a potential trough in the channel between the adjacent buckets which may trap carriers during transfer and reduce CTE. The effect of the gap can be ameliorated either by reducing the gap size, increasing the clocking voltages, adding a fat-zero signal, or recessing the dielectric in the gap region. The gap size must be ultra small in the 2DEG-CCD, comparable to the dielectric thickness (30 nm), and may be achieved in III–V technology through the use of anodized or oxide isolated, overlapping gates. Thus far, this technology has only been explored for MESFET-type GaAs CCD's [16], [17], but should also be applicable to 2DEG-CCD's. Advanced lithographic techniques may also be used to define ultra-small gap sizes. Increasing the clocking voltages is undesirable because of gate-to-gate breakdown, increased power dissi-

pation, and excess dark current. The addition of a fat-zero can increase noise in many applications and also reduces dynamic range. The recessed-gap technique [18] is most effective in uniformly doped dielectric structures since fixed charge is removed during the recess process. In the case of planar-doped structures, the recess has been found to reduce gate-to-gate leakage and dark current [19].

The RG approach to electrode design eliminates gap fabrication problems and CTE loss due to potential troughs. Gate-to-gate breakdown is also avoided. The drawback of the RG approach is the dissipation of dc power in the gates due to current flow between adjacent finger electrodes. However, at high frequencies, this power dissipation is typically less than that induced in CG approaches due to gate-to-gate parasitic capacitance in the latter. At low frequency, the sheet resistance of the RG material can be chosen to reduce power dissipation to modest levels. For imager applications, a two-phase RG electrode design [20] described below can be used to eliminate dc power dissipation during frame integration. Another advantage of the RG approach for imagers is that the metallic electrode surface coverage is less than in the CG approach, thus enhancing fill-factor for frontside illumination without resorting to transparent metal (e.g., ITO [21]) technology.

### B. Charge Capacity

Calculation of the charge in the channel using one-dimensional analysis may be found in Shur [1], and is performed here using a more simplistic formalism which nonetheless is in reasonable agreement with more complex calculations. First, let the barrier height between the gate and dielectric be $q\phi_b$, and the heterojunction discontinuity be $q\phi_d$ (see Fig. 2(b)). In equilibrium, let the channel Fermi level be $q\phi_f$ above the conduction band edge, so that the built-in voltage $V_{\text{bi}}$ is given by

$$V_{\text{bi}} = \phi_b - \phi_d + \phi_f. \tag{1}$$

Without fixed charge in the dielectric there is no channel charge with zero gate bias and $\phi_f$ is negative. With a fully depleted, n-doped dielectric, there can be charge in the channel (a normally "on" configuration). Assume the dielectric has fixed charge given by $\rho(x)$ and define the areal gate capacitance as

$$C_g \triangleq \epsilon_0 \epsilon_s / (d + \Delta d) \tag{2}$$

where $\epsilon_0$ is the permittivity of free space, $\epsilon_s$ is the relative dielectric constant of the insulator, $d$ is the insulator thickness, and $\Delta d$ is a quantum effect correction factor, and is typically 5–10 nm. The areal charge in the channel at zero bias is then

$$Q_{s0} = -\int_0^d \rho(x)[x/(d + \Delta d)]\, dx + C_g V_{\text{bi}} \tag{3}$$

where it is assumed that $Q_{s0} < 0$ and $x$ is taken to be zero at the gate–dielectric interface. It can be seen that the fixed charge in the dielectric is most effective in producing channel charge if located close to the heterojunction. With applied bias $V_g$, the channel charge becomes

$$Q_s = Q_{s0} - C_g V_g \tag{4}$$

assuming the channel potential remains at zero. In a CCD, gate voltage is often fixed, and the channel charge variable. In this case, the channel potential $V_c$ is given by

$$V_c = V_g - (Q_{s0} - Q_s)/C_g \tag{5}$$

with a maximum value $V_m = V_g$ for no channel charge. As with other CCD technologies, if not blocked by a potential barrier, the channel charge will flow to the "bucket" with the most positive potential. Note that the bucket potential swing between full and empty is relatively small, just $Q_{s0}/C_g$ which is typically of the order of 0.5–1.0 V due to the high value of $C_g$. However, this also indicates that the required clock swing is commensurately low, an important factor in power dissipation.

The charge capacity of the 2DEG-CCD, due to its surface channel configuration is determined by the maximum allowed leakage current through the dielectric. Under enhancement conditions (positive bias), the channel is forward-biased with respect to the gate, and a forward-bias current will flow. However, for small forward biases, this current is comparable to the empty bucket dark current and can be ignored, thus extending the possible voltage swing on the gate and consequent charge handling capability. In this paper, the enhancement operation is not considered due to the delicate biasing required. The areal charge handling capacity is simply $Q_{s0}$, and the minimum clock swing required to transfer this charge $V_{mcs}$ is

$$V_{mcs} = Q_{s0}/C_g \tag{6}$$

and as indicated above, can be quite small.

In a CG structure, the maximum charge capacity is just the areal charge capacity multiplied by the electrode area. In an RG structure, the calculation is complicated by the voltage-divided potential well shape. Assuming the one-dimensional analysis continues to be valid (a gradual channel approximation), the capacity of the RG structure can be calculated as follows. Let the finger electrode geometry have width $w$ and length $l$, and let the finger spacing be $s$, yielding a four-phase pixel area of $4w \cdot (l + s)$. For low-frequency clocking such that the square-wave nature of the clock voltage waveforms (of swing $V_{cs}$) is preserved at the pixel, the charge is confined to a length of $s + 2(l + \Delta s)$, where $\Delta s$ is given by

$$\Delta s = (V_{mcs}/V_{cs}) \cdot s \tag{7}$$

leading to a maximum charge handling capacity of

$$Q_{\max} = Q_{s0} w[2l + (1 + V_{mcs}/V_{cs})s]. \tag{8}$$

At high frequency, the clock waveforms appear sinusoidal at the pixel, and the charge handling capacity is reduced to $Q'_{\max}$ given by

$$Q'_{\max} = Q_{\max} - Q_{s0} ws. \tag{9}$$

Thus there is a tradeoff in the use of the RG structure for a given pixel size in that small $s$ increases charge capacity but decreases the electrode-to-electrode resistance, thereby increasing power dissipation. Larger $l$ also increases the flat-field region for charge transfer, decreasing the high-frequency performance of the device.

### C. Dielectric

The doping and thickness of the dielectric is critical in determining some of the most important characteristics of the 2DEG-CCD. When uniformly doped (MODFET-type CCD), small changes in dielectric thickness can dramatically change the channel charge, pinch-off voltage, and gate leakage current. The band diagram for this type of gate structure is shown schematically in Fig. 3(a). While this structure was the basis of initial experiments on 2DEG-CCD's due to the relative ease of material growth, it performs the most poorly with respect to CTE and dark current. The dark current, described more fully below, is increased by the high field at the gate–dielectric interface. The CTE is reduced by trapping in the AlGaAs. The low temperature (e.g., 10 K) performance of the device is also degraded due to the partial freeze-out of the dielectric dopant impurities.

A more recent alternative to uniform doping is the use of a planar doping layer, as illustrated in Fig. 3(b). The thickness of this layer is typically under 1 nm, and could be as thin as a single atomic plane ($\delta$-doping). The effective doping concentration in this layer can be very high, $10^{19}$–$10^{20}/\text{cm}^3$. This has three major effects. First, the dopants can be placed close to the heterojunction where they are the most effective in producing channel charge, increasing the CCD bucket capacity. Second, for the same channel charge, the field at the gate–dielectric interface is reduced, exponentially decreasing dark current. Third, the degenerately doped layer is more immune to freeze-out effects than the uniformly doped dielectric, thus improving operation at very low temperature.

If the doping distribution in (3) is insufficient to produce channel charge at zero bias, sufficient positive gate bias may be able to attract electrons to the heterojunction and thereby enable the device to operate in an enhancement mode. As an extreme example, the undoped dielectric case is considered, as shown in Fig. 3(c). This FET structure, also known as the heterojunction insulated gate FET, or HIGFET, or with a semiconductor gate, SISFET, has several advantages, and one large disadvantage. The advantages are that the voltage required to create the channel (i.e., threshold voltage) is less dependent on the dielectric thickness and doping uniformity across a wafer, easing digital circuit design and MBE requirements. Furthermore, there is no doping layer to freeze out during cryogenic operation. The major disadvantage is that dark current is greatly increased since the barrier limiting electron emission from a full well is the band offset at the heterojunction, typically much smaller than the barrier at the gate–dielectric interface. Thus only very high speed applications in which short charge packet residency times are required may be able to utilize this undoped dielectric technology until a depletion-mode device is formed.

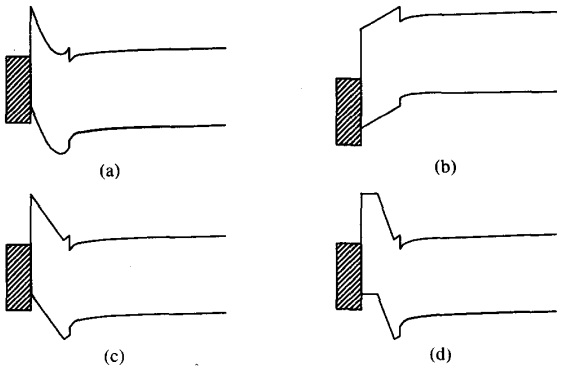



Fig. 3. Band diagrams for four possible dielectric doping conditions. (a) Uniform doping. (b) Planar doping. (c) Undoped dielectric (with positive bias on gate). (d) p-i-n-doped dielectric. In each case, the same quantity of channel charge is illustrated.

It is also possible to devise an inverted 2DEG-CCD structure, similar to an inverted HEMT technology [22]. In this case, the order of material layers is reversed, with doped dielectric material under the heterojunction, and the gate placed on the channel material. While this solved some early HEMT technology problems, particularly related to AlGaAs, it may lead to reduced charge capacity in a CCD.

While not discussed, it should be kept in mind that the entire 2DEG-CCD structure can be recast as a 2DHG (hole gas) structure, by inverting the doping polarity, and changing the appropriate signs in (1)–(4). A 2DHG-CCD may be appropriate for the monolithic integration of a HIP-type detector, in which holes are emitted over an internal photoemission barrier, and collected by the CCD bucket. The 2DHG mobility is also high, and most of the attributes of the 2DEG-CCD apply to the 2DHG-CCD as well.

### D. Materials

The choice of gate material affects device parameters through the barrier height $\phi_b$ and is chosen to maximize the barrier height while preserving device manufacturability and reliability. A good choice for the AlGaAs/GaAs system is Cr and Au successive metallization, which provides a high barrier to AlGaAs, and which maintains good adhesion and high conductivity. For RG applications, cermet [8], [9] has been used. It has been observed that cermet-gate devices have lower dark current than Cr/Au devices by approximately one order of magnitude, which is attributed to the microstructure of cermet. The latter is believed to consist of microscopic clusters of Cr embedded in a $SiO_x$ matrix, thus leading to an effective reduction of the Cr contact area at the surface. An alternative to cermet is the use of a semiconductor material whose doping and thickness are chosen to provide sufficient sheet resistance. The advantages of a semi-

conductor resistive gate are that it may be grown *in situ* during growth of the underlying structure thus eliminating a later deposition process, it is (generally) lattice-matched with good adhesion, and perhaps most importantly, offers an intriguing opportunity to consider HIP-type devices intimately integrated into the gate structure. The semiconductor gate suffers from an important disadvantage as well. The semiconductor gate, unlike a metallic gate, has a slower dielectric response time, thus inhibiting rapid charge transfer under the gate. Increasing the carriers in the gate cannot be done without lowering the sheet resistance. This discussion will be presented more thoroughly by Rossi *et al.* [15].

Two primary material systems are being presently pursued for the 2DEG-CCD. The first, and most mature, is the AlGaAs/GaAs system, and the second is the InAlAs/InGaAs/InP system. Other systems using II–VI and VI–VI material heterojunctions might also be considered but have not yet been explored. A silicon-based 2DEG-CCD technology would be of interest because of potential compatibility with silicon-based processing. The AlGaAs/GaAs system is shown schematically in Fig. 4(a). The Al mole fraction is usually chosen to be 30%, yielding a bandgap of 1.85 eV, and a conduction band offset of 0.27 eV. The barrier height of Cr on $Al_{0.3}Ga_{0.7}As$ has been measured to be 0.935 eV [4]. With a bandgap of 1.42 eV, the cutoff wavelength for direct optical absorption in the GaAs channel is 0.87 $\mu$m. Enhanced short-wave infrared (SWIR) response can be obtained in the InAlAs/InGaAs/InP system due to the germanium-like bandgap of lattice-matched InGaAs, shown schematically in Fig. 4(b). To achieve lattice matching to the InP substrate, the alloy compositions are chosen to be $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$, yielding respective energy gaps of 1.48 eV and 0.76 eV corresponding to a channel absorption cutoff wavelength of 1.63 $\mu$m. The conduction band offset is 0.48 eV. Since the InP bandgap is 1.35 eV, it is transparent to the SWIR and backside illumination can be used without backside thinning.

The choice of material system depends upon the ultimate application of the 2DEG-CCD. For detector readout, detector material compatibility is the most important factor. For high-speed applications, the channel mobility plays an important role, but at the present time, the high-speed limits of these devices are beginning to be explored by PISCES modeling at 40 GHz [19], with experimental results not yet attained beyond 1 GHz. Manufacturability is another factor in material choice. The AlGaAs/GaAs system is being pushed by digital circuit applications, and the InAlAs/InGaAs/InP system pushed by optoelectronic (e.g., fiber optic communication) applications.

### *E. Dark Current*

Dark current in III–V devices is typically larger than that found in silicon CCD's despite the large energy bandgap of the former. The dominant reason for this is that III–V CCD's do not enjoy the benefit of the high gate–$SiO_2$ dielectric interface barrier height, and thermionic

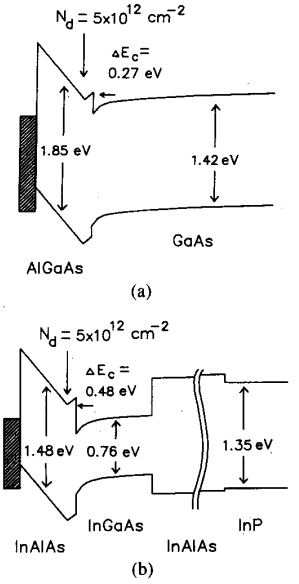



Fig. 4. Band diagrams for (a) $Al_{0.3}Ga_{0.7}As/GaAs$ material system and (b) $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/InP$ material system.

emission (TE) over the lower barrier leads to dark current exceeding the band-to-band and heterointerface generation mechanisms. In the case of the 2DEG-CCD's with high electric fields at the gate–dielectric interface, thermionic field emission (TFE) in which quantum-mechanical tunneling into the dielectric conduction band occurs, can result in still higher dark current.

For an empty bucket, the TE component of dark current $J_{TE}$ can be modeled as

$$J_{TE} = A^{**}T^2 \exp(-q\phi_b/kT) \tag{10}$$

where $T$ is the temperature, $A^{**}$ is the effective Richardson constant, and $\phi_b$ the gate–dielectric interface barrier height. The TFE component of dark current $J_{TFE}$ [23] contains the tunneling probability $T(E_z)$ given as

$$T(E_z) = \exp\{(-4\pi/h)\int_{x_1}^{x_2}\{2m^*[qV(x) - E_z]\}^{1/2}\,dx\} \tag{11}$$

where $m^*$ is the effective electron mass in the dielectric, $E_z$ the perpendicular component of electron energy, and $x_1$ and $x_2$ are the classical turning points. The potential $V(x)$ includes image force lowering and is given in turn by

$$V(x) = \phi_b - q/16\pi\epsilon_0\epsilon_s x + \int_0^x E(x')\,dx' \tag{12}$$

where $E(x)$ is the electric field in the dielectric. The TFE current density is then

$$J_{TFE} = 1/2\int_0^{\phi_b} qv_z(E_z)T(E_z)\int_0^{\infty} f(E_z + E_{xy}) \cdot \{(8\pi/h^3)m^*[2m^*(E_z + E_{xy})]^{1/2}\}\,dE_{xy}\,dE_z \tag{13}$$

where $\phi_b'$ is the barrier height modified by the image-force barrier lowering, $f(E)$ is the Fermi–Dirac distribution function, $V_z$ the perpendicular electron velocity, and $E_{xy}$ the electron energy parallel to the interface. The TFE component is less dependent on temperature compared to the TE component, indicating that cooling the 2DEG-CCD will not easily suppress dark current if TFE dominates.

Since the TFE component depends critically on the field in the dielectric, reduction of the field at the gate–dielectric can significantly affect dark current. A tailored approach to dielectric doping can reduce the field. The use of a p-i-n doped gate, as illustrated in Fig. 3(d), can restore the dark current to TE-limited operation at room temperature, and shift the crossover point to TFE operation to lower temperatures. A comparison of these expressions and experimental results are presented in Fig. 5.

Other sources of dark current include thermal generation in the channel, $J_{CG}$ and thermal generation at the heterojunction $J_{HG}$. These currents are, respectively, given by

$$J_{CG} = qn_iW/2\tau \tag{14}$$

and

$$J_{HG} = qn_is_0 \tag{15}$$

where $W$ is the thermal collection depth of the channel, $\tau$ is the minority carrier lifetime, and $s_0$ is the surface recombination velocity at the heterojunction. For GaAs with a room temperature $n_i$ of $1.8 \times 10^6/\text{cm}^3$, $W$ of 1 $\mu$m, $\tau$ of the order of 10 ns, and $s_0$ of 10 cm/s (chosen for illustrative purposes) the channel and heterojunction components are 1.4 $\text{nA/cm}^2$ and 0.3 $\text{pA/cm}^2$, respectively. This can be compared to observed room temperature TFE currents in uniform-doped and planar-doped 2DEG-CCD's of 3 $\text{mA/cm}^2$ and 20 $\mu\text{A/cm}^2$, respectively.

The dark current determines the maximum residency time of a charge packet in the CCD. Typically, the integrated dark current should be no more than 0.1–0.01% of the full-well capacity. The maximum residency time $t_{\max}$ is found by dividing the maximum allowable integrated dark current by the dark current. For a delay line application, the minimum operating frequency $f_{\min}$ is simply $M/t_{\max}$, where $M$ is the number of stages in the delay line. In an imager, $t_{\max}$ corresponds to approximately twice the frame integration time.

### *F. Charge Transfer*

The large low-field mobility of 2DEG devices (5000–10 000 $\text{cm}^2/\text{V}\cdot\text{s}$ at 300 K, 20 000–200 000 $\text{cm}^2/\text{V}\cdot\text{s}$ at 77 K) enables high-frequency operation of the 2DEG-CCD. The transfer time for a CG device can be estimated using techniques developed for silicon MOS CCD's [24], [25]. Self-induced drift will govern the initial stages of charge transfer, followed by diffusion in the case of long gate lengths, or fringing-field drift in the case of short gate lengths (e.g., $< 1$ $\mu$m). A characteristic time constant for self-induced drift is approximately

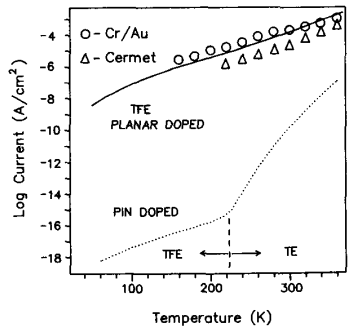



Fig. 5. Logarithmic plot of maximum gate current density (dark current) as a function of temperature for both planar-doped and pin-doped dielectrics. Experimental data are shown by symbols; solid curve is theoretical model for thermionic field emission (TFE), dotted curve is thermionic emission (TE) and TFE components for pin-doped dielectric ($m^* = 0.080\ m_0$).

$$\tau_{\text{sid}} = 2L^2/\pi\mu V_{mcs} \tag{16}$$

where $L$ is the transfer length. Using a mobility of 5000 $\text{cm}^2/\text{V}\cdot\text{s}$, $L = 4$ $\mu$m, and $V_{mcs} = 1$ V, the characteristic time is 20 ps. The thermal diffusion time constant $\tau_{\text{dif}}$ is

$$\tau_{\text{dif}} = (q/kT)(2L/\pi)^2(1/\mu) \tag{17}$$

which corresponds to 500 ps. Thus large CG 2DEG-CCD's can still yield very high transfer speeds (in this case 50 MHz for a 4-phase device with 0.9999 CTE).

Resistive-gate devices are much faster than capacitive-gate devices when the transfer length exceeds a few micrometers. Initially, charge transfer is still limited by self-induced drift, but as the potential well is uncovered, the built-in lateral field accelerates transfer of the remaining charge. Thus the transfer time is roughly the sum of the self-induced drift time of (16) plus the single-carrier transit time. The single-carrier transit time is simply

$$\tau_{\text{tr}} = L^2/\mu V \tag{18}$$

where $L \approx s$ and $V$ is the difference in potential between the two buckets. (If $V$ is sufficiently large, an additional effect—the inhibition of charge packet broadening [26] may also occur.) The RG transfer time is thus

$$\tau_{\text{rg}} = (L^2/\mu V)[1 + (2/\pi)(V/V_{mcs})] \tag{19}$$

which for the parameters above and $V = V_{mcs}$ is 52 ps, corresponding to a 4-phase maximum clocking rate of approximately 5 GHz. For RG devices with large finger widths $l$, the charge transfer time becomes dominated by the slow process in the resultant "flat" region, and the CG characteristic times apply.

For a RG device operating at high frequency, the sheet resistance must be chosen to assure that the interelectrode region follows the applied potential. Thus the transmission line equivalent delay time must be less than the clocking period. A characteristic time for charging the resistive gate is

$$\tau_{\text{rc}} = (\pi/8)R_{\square}C_gs^2. \tag{20}$$

Since this time must be approximately less than or equal to the carrier transit time, an upper bound on the resistivity of the gate material is obtained as

$$R_{\square} \leq 8/(\pi\mu C_g V_{cs}). \tag{21}$$

For the parameters used above, this is 1700 Ω/□ for 5 GHz assuming a minimum clock swing. Typically, high-frequency clock lines are designed to be terminated with 50 Ω, placing a limitation on either the geometry of each stage of the delay line, or the total number of stages.

The power dissipated in the resistive gate of an $M$-stage four-phase delay line with finger electrodes spaced by $s$ and channel width $W$ is simply

$$P = 2M(w/s)V^2_{cs}/R_{\square} \tag{22}$$

and halved if driven by sinusoidal clocking waveforms. It should be noted that for imaging applications, $R_{\square}$ for the gate material can be very high (> 1 GΩ/□) to minimize power dissipation, with charge transfer speed limited by resistive-gate charging time. For example, a 512 × 512 imager with a 1-GΩ/□ resistive gate could operate at 50 kpixel/s with a gate power dissipation of 12 μW.

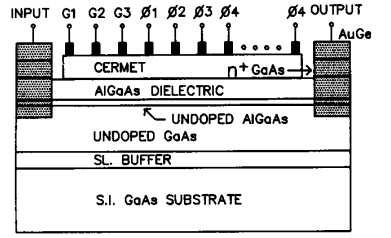
Transfer efficiency limitations in 2DEG-CCD's are not presently well understood. While traps at the heterointerface are expected to be of low density, these traps would contribute to a loss in CTE. Bulk traps in the channel layer or dielectric may also contribute. However, experimentally, CTE seems to not be a strong function of frequency or operating temperature, indicating that traps are not presently dominating CTE. A more likely explanation is that carriers are injected into the dielectric layer where they have lower mobility and are confined by a parasitic potential well (as seen in Fig. 3(a)) within doped dielectric. An undoped dielectric configuration would remove this effect. Investigation into the fundamental CTE limitations is underway.

## III. Experimental Results

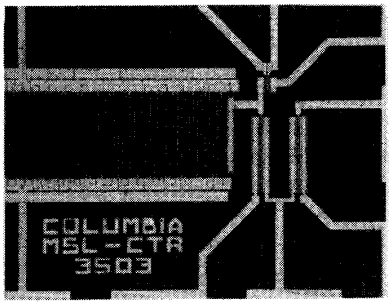
Experimental results for several 2DEG-CCD configurations are reviewed. A uniform-doped and planar-doped $Al_{0.3}Ga_{0.7}As/GaAs$ 2DEG-CCD are compared with respect to dark current and consequent low-frequency operation limits. A two-phase resistive-gate 2DEG-CCD utilizing a recessed gate is described which does not require power dissipation in the gate during frame integration.

### A. Uniform-Doped AlGaAs/GaAs 2DEG-CCD

A schematic diagram of the resistive-gate 2DEG-CCD is shown in Fig. 6(a). The material was grown at Columbia University with a Varian Gen-II molecular beam epitaxy (MBE) system on a ⟨100⟩ semi-insulating GaAs substrate. The structure, from bottom to top, consists of a GaAs/AlGaAs superlattice buffer, a 500-nm-thick undoped GaAs layer, a 3-nm-thick undoped AlGaAs spacer layer, a 35-nm-thick AlGaAs layer doped with 2 × $10^{18}/cm^3$ Si atoms, and a 30-nm-thick GaAs cap layer doped with 4 × $10^{18}/cm^3$ Si atoms.




(a)




(b)

Fig. 6. A four-phase, resistive-gate 2DEG-CCD delay line. (a) Cross section. (b) Chip photograph.

After a 400-nm-deep mesa etch using 1:1:200 $NH_4OH:H_2O_2:H_2O$, AuGe ohmic contacts were formed and annealed at 425°C for 45 s under a forming gas ambient. Using the AuGe ohmic contact pattern as a mask, the 30-nm GaAs cap layer and 5 nm of the $n^+$-AlGaAs layer were etched with a 1:1:1000 $NH_4OH:H_2O_2:H_2O$ solution. A resistive layer (cermet) was e-beam evaporated on the CCD channel with an equal weight mixture of Cr and SiO powder sources [9], forming a Schottky contact to the underlying $n^+$-AlGaAs layer. The resistive layer was 250 nm thick with a sheet resistance of 350 kΩ/□. The first Cr(5 nm)/Au(200 nm) metallization was done by e-beam and filament evaporations, respectively, to form finger electrodes on the resistive layer and gate electrodes for the output amplifier. A 350-nm-thick SiO layer was e-beam evaporated to serve as an intermetal dielectric layer and lifted off to form via holes. The second Cr(5 nm)/Au(300 nm) metallization was used to connect finger electrodes with the same phase. All deposited layers were defined by a standard lift-off process.

During the fabrication, the dc characteristics of a FET were monitored. A degradation of transconductance and saturation current was observed whenever the AlGaAs layer between the gate and the source or the drain region was exposed to the developer for consecutive process steps. This was attributed to the etching of the AlGaAs layer in the developer (Shipley Microposit Concentrate mixed 1:1 with DI water). The inadvertent etching rate was measured to be about 1 nm/min.

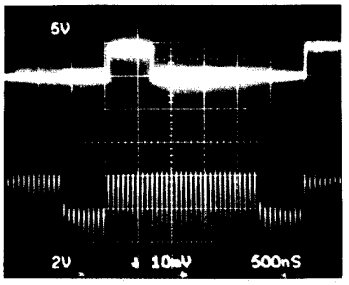
The CCD delay line is composed of 32 stages with a four-phase clocking scheme (128 electrodes). The finger

electrodes are 1 $\mu$m long, 100 $\mu$m wide, and spaced by 4 $\mu$m. An on-chip output amplifier composed of two MODFET's with 1 $\mu$m long by 100 $\mu$m wide gates configured as a source-follower with active load and a dual-gate reset MODFET is used to read out the signal from the CCD channel. The completed chip is shown in Fig. 6(b).

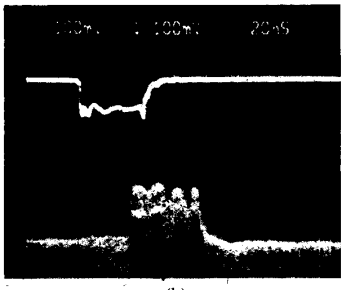
Before operating the CCD delay line, basic device characterization was performed. As determined by a Hall effect measurement, the electron mobility was 4300 $cm^2/V \cdot s$ at 300 K, 20 000 $cm^2/V \cdot s$ at 77 K, and the sheet carrier density $n_{s0}$ was $1.5 \times 10^{12}$ electrons/$cm^2$. The pinch-off voltage of the normally-on CCD channel was $-0.8$ V determined by a capacitance–voltage measurement. The transconductance of a 1-$\mu$m gate FET was measured to be 100 mS/mm. This relatively low transconductance is attributed to the source resistance since the amplifiers were not fabricated by a self-aligned process. The room-temperature leakage current density of the CCD channel was typically 2 $mA/cm^2$ at a reverse bias near the pinch-off voltage.

The operation of the CCD delay line was performed at low and high frequencies. The low-frequency test was done at clock frequencies up to 13 MHz which was the maximum available with the low-frequency test station. Fig. 7(a) shows the input and the delayed output signal at 13-MHz clock frequency at room temperature, corresponding to a CTE of better than 0.999, as evaluated using the method of Brodersen *et al.* [27]. The CTE at lower frequencies degraded rapidly; for example, at 1.5-MHz clock frequency the CTE was 0.98 and the output signal became smaller. Both results are attributed to the gate leakage into the CCD channel. A simple calculation shows that the integrated dark-current signal begins to exceed the maximum charge handling capability of the bucket at this low frequency. The signal amplitude and the CTE improved as the device was cooled, suggesting that the dark current indeed sets the low-frequency limit.

The high-frequency test was done for clock frequencies between 600 MHz and 1 GHz (the range of the test station). The test result at 1-GHz clock signal at room temperature is shown in Fig. 7(b). Note that the output signal closely follows the ringing of the input signal. No degradation of the CTE up to 1-GHz operation was observed. The output signal amplitude increased compared with that of the low-frequency operation despite the decreased gain of the output amplifier due to 50-$\Omega$ loading by the sampling oscilloscope. Although not fully understood, it may be related to the dark current.




(a)



(b)

Fig. 7. Input and output waveforms for a 32-stage uniform-doped RG 2DEG-CCD delay line at (a) 13 MHz and (b) 1 GHz. In the latter, note that ringing of input pulse is faithfully sampled by the CCD, as seen in sampling oscilloscope waveform envelope. CTE is approximately 0.999 for (a) and (b).

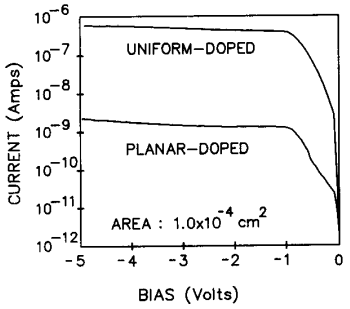



Fig. 8. Comparison of measured reverse-bias gate leakage current measurements for uniform-doped and planar-doped devices.

### *B. Planar-Doped AlGaAs/GaAs 2DEG-CCD*

The material structure for the planar-doped 2DEG-CCD consists of, from bottom to top, a semi-insulating GaAs substrate, a GaAs/AlGaAs superlattice buffer, an 800-nm-thick undoped GaAs layer, a 3-nm-thick undoped AlGaAs spacer layer, a planar-doped AlGaAs layer ($4.5 \times 10^{12}$ Si atoms/$cm^2$), a 35-nm-thick undoped AlGaAs layer, an a 30-nm-thick GaAs cap layer doped with $4 \times 10^{18}/cm^3$ Si atoms. Fabrication is similar to that of the uniform-doped device except that 10 nm of AlGaAs was removed, and the resistive gate was 300 nm thick with a sheet resistance of 250 k$\Omega/\square$.

The same mask as described above was used to define the delay line. Before operating the CCD, basic device characterization was again performed. The pinch-off voltage and transconductance of a 1-$\mu$m gate-length FET were $-1$ V and 100 mS/mm, respectively. The gate leakage current of the planar-doped structure was measured to be more than two orders of magnitude lower than that of a uniform-doped structure at room temperature as shown in Fig. 8. The CTE of this device is plotted in Fig. 9 in comparison with that of the uniform-doped CCD, which shows an extended low-frequency limit by a similar factor as the gate leakage reduction. The improvement in CTE

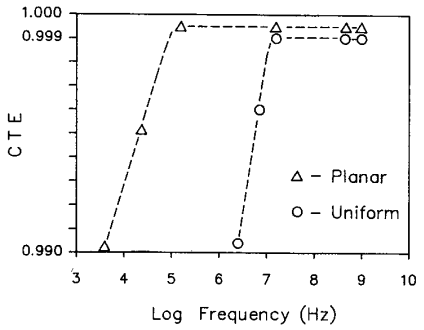



Fig. 9. Comparison of CTE between uniform-doped and planar-doped 2DEG-CCD's as a function of frequency.

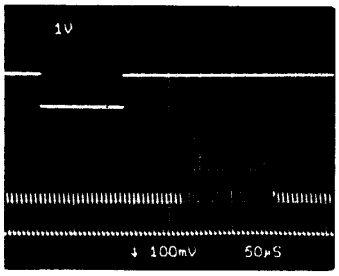



Fig. 10. Input and output waveforms for a 32-stage planar-doped 2DEG-CCD at low frequency (133 kHz) showing improved low-frequency performance due to dark current reduction.

is thought to be due to the reduction of the AlGaAs parasitic potential well (see Fig. 3). Fig. 10 shows the operation of the planar-doped CCD delay line at a 130-kHz clock frequency at room temperature, corresponding to a CTE of 0.9997.

### C. Two-Phase Uniform-Doped AlGaAs/GaAs 2DEG-CCD

A schematic illustration of the two-phase device is shown in Fig. 11(a). The major difference between the two-phase and four-phase device structures is that a recessed gate is defined and deposited prior to cermet deposition. Recessing reduces the depth of the potential well under the recess [18], [28], [29]. In the two-phase device, the finger electrodes are spaced and connected as shown in Fig. 11(b) yielding the illustrated potential well diagrams. With equal bias applied to phases 1 and 2, note that every half-pixel has its potential well isolated without the need for power dissipation in the resistive gate. With sufficient bias, the barrier between half-pixels is suppressed and charge can be transferred in the channel. The recess-induced potential continues to inhibit the back propagation of charge and allow two-phase operation.

The starting material was the same as that used in the uniform-doped four-phase structure above, with similar dark current limitations. The recess was performed by wet etching using a photoresist mask to a depth of 10 nm, followed by Cr–Au metallization and liftoff, resulting in a self-aligned recessed gate. The potential barrier induced

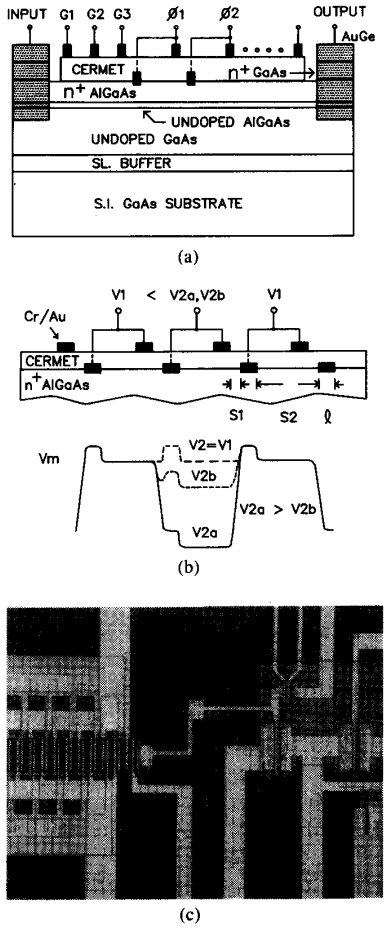



Fig. 11. A two-phase, resistive-gate 2DEG-CCD delay line. (a) Material layers. (b) Electrode configuration and resultant potential wells ($l$ = 2 $\mu$m, $s_1$ = 1.5 $\mu$m, $s_2$ = 6.5 $\mu$m). (c) Chip photograph.

by the recess was measured to be 1.0 V yielding a charge handling capacity of $1.5 \times 10^{12}/\text{cm}^2$ carriers. The cermet was 400 nm thick with a resistivity of 450 k$\Omega/\square$. The CCD was organized as a 38-stage delay line with a 24 $\mu$m × 24 $\mu$m pixel. The output amplifier included an integrated on-chip 2DEG-FET load. A photograph of the two-phase 2DEG-CCD is shown in Fig. 11(c).

At the test station limit of 26 MHz, the highest CTE was obtained, and was measured to be 0.9993 at room temperature. Input and output waveforms are shown in Fig. 12. As expected, degradation of the CTE was observed at clock frequencies lower than 20 MHz due to dark current. The CTE dependence on clock voltage swing is shown in Fig. 13. In order to suppress the 1-V barrier induced by the recess, a minimum 6-V clock swing was required.

The two-phase device is expected to find application in systems which require increased simplicity in clock voltage drive. The charge fill-factor (fraction of pixel area available for charge storage) is also increased over the four-phase device, and is not diminished by sinusoidal

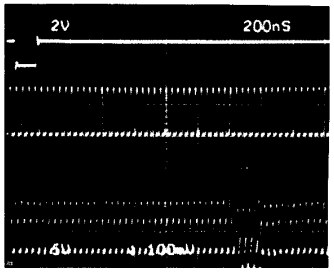



Fig. 12. Input and output waveforms for a 38-stage two-phase 2DEG-CCD delay line at 26 MHz. Upper trace is input, middle trace is clock waveform, and lower trace is output. CTE is 0.999.

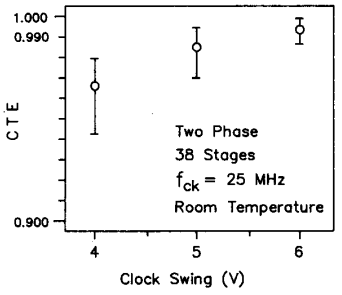



Fig. 13. CTE as a function of clock voltage swing for the two-phase 2DEG-CCD measured at 25 MHz.

clocking. The electrode design also allows for optical illumination of the pixel with good optical fill-factor, should direct detection be utilized.

## IV. Discussion and Summary

The 2DEG-CCD shows significant promise in addressing both high-speed and IR detector multiplexing applications. The 2DEG-CCD features high charge handling capacity, low-temperature performance, high-speed charge transfer, and potentially low-interface trap noise. While still in its infancy, the technology has readily demonstrated performance and reproducibility. Improvement in both dark current reduction and charge transfer efficiency remains to be developed, but the margin for such advancement is large. Unlike its digital counterpart, threshold nonuniformity in III-V 2DEG-CCD structures is not critical, and this technology is not expected to be stymied by this traditional III-V material limitation.

In summary, AlGaAs/GaAs 2DEG-CCD's have been shown to operate with 0.9997 charge transfer efficiency, at frequencies ranging from 130 kHz to 1 GHz. Operation at higher frequencies has not been explored to date due to test station limitations. A review of fundamental principles of operation and a discussion of structural and material configurations have been presented.

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